High-Efficiency Bridgeless Flyback Rectifier With Bidirectional Switch and Dual Output Windings

Jong-Won Shin, *Member, IEEE*, Sung-Jin Choi, *Member, IEEE*, and Bo-Hyung Cho, *Fellow, IEEE*

***Abstract*—This paper proposes and analyzes a new bridgeless flyback power factor correction rectifier for ac–dc power conversion. By eliminating four bridge diodes and adding a few circuit elements, the proposed rectifier reduces the primary side conduction loss and improves efficiency. The addition of the new elements has minimal effect on the circuit simplicity because it does not need any additional gate driver and magnetic elements. The losses in the semiconductor devices of the proposed circuit are analyzed and compared with that of the conventional one, followed by transformer design guideline. Experimental results with the practically implemented prototype prove its higher efficiency than its conventional counterparts.**

***Index Terms*—Bridgeless rectifier, high efficiency, flyback converter, power factor correction (PFC).**

I. Introduction

FLYBACK converter has been an attractive solution in various power conversions due to its topological advantages such as simple structure, low cost, and galvanic isolation. It is utilized as power factor correction (PFC) ac–dc rectifier and dc–ac inverter where the harmonics of line current are regulated. In these applications, no in-rush current and easily achievable high power factor (PF) by simple control [1] act as another good features of the flyback converter. Due to these advantages, the flyback circuit is widely used in light emitting diode driver [2]–[4] and microinverters [5]–[7].

However, improving the efficiency of the flyback converter is not straightforward. It suffers from high current stress in semiconductor devices and circulating energy between transformer leakage inductance and primary switch parasitic capacitance. The degraded efficiency consequently limits the flyback topology to low-power range smaller than a few hundred watts.

Many researchers have improved the efficiency of the flyback converter. One of the famous approaches is actively clamping the main switch on the primary side [8]–[10], which replaces resistive snubber [11]. The clamp circuit, whether it is connected parallel with the transformer primary winding or the main switch [12], [13], absorbs the energy stored in the leakage inductance and recovers it to the input side. This method requires additional capacitor, switch, and its driver instead of achieving low voltage stress across the main switch and high efficiency of the converter. Other lossless snubbers for the flyback converter have already been reported [14], [15]. In [14], inductor of the conventional nondissipative LC snubber [16] is replaced by an additional winding of the transformer. However, its performance is sensitive to the leakage inductance and the efficiency increase is not remarkable compared with the conventional one. In [15], an active switch and two more additional windings as well as the other passive elements increase the circuit complexity. Another approach for flyback converter efficiency improvement is the soft switching to reduce switching loss of the main switch. Quasi-resonant switching [17] maintains the minimum drain–source voltage of the main switch at turn-on instant to minimize the switching loss. Nevertheless, it requires additional voltage detection circuit to find the switching instant during the resonant period, and its variable frequency operation degrades PF. Zero voltage switching schemes are also presented in [18] and [19], by utilizing an additional magnetic element.

Besides the active clamping and soft switching techniques, bridgeless rectifier concept is a special and effective way to increase the efficiency of the ac–dc power conversion. It removes the bridge diodes on the rectifier input side to eliminate their conduction loss. Furthermore, the bridgeless rectifier demonstrates the same frequency dynamics with the conventional rectifier so that the conventional control loop design can be applied without significant change. Its application to the boost rectifier is well presented and experimented in [20], as well as to the buck [21] and flyback rectifier [22]–[24]. One common drawback of the bridgeless rectifier is that its part count is almost twofold of its counterpart circuit: the bridgeless rectifier effectively uses two converters, one for the positive half-line cycle and another for the negative cycle. In particular, using more than one magnetic device in the flyback rectifier [18], [19], [22], [23] severely harms the circuit simplicity which is the most important advantage of the flyback converter. Modified flyback converter presented in [24] does not have another transformer, but the two main switches on the primary side use their own gate drivers and make the rectifier complicated because they share neither their source terminals nor gate signals.

This paper articulates the bridgeless flyback rectifier presented in [25]. It is with no bridge diodes to remove the diode conduction loss and improve the rectification efficiency, and the part count increase in the other part of the circuit is minimized

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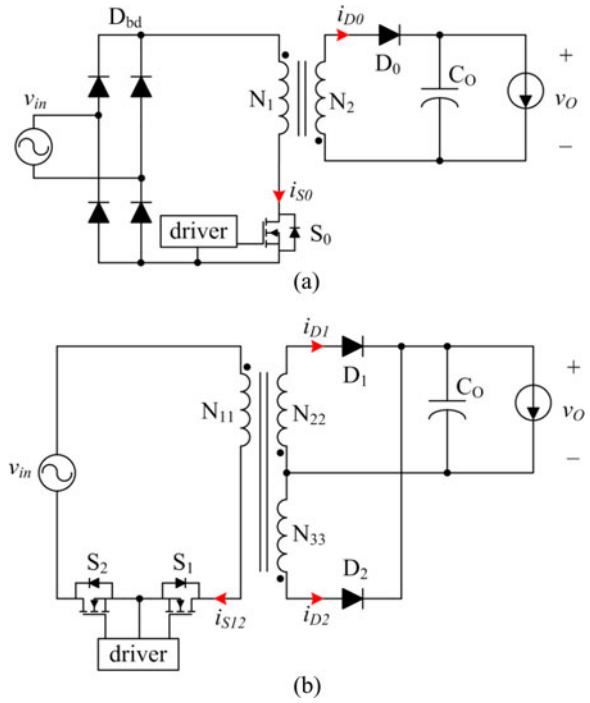

Fig. 1. Circuit configuration of (a) conventional and (b) proposed flyback rectifier.

to preserve the simplicity of the flyback converter. The proposed circuit only introduces a switch, a diode, a winding in the transformer, and no magnetic element as the additional circuit components. The additional switch shares the same gate signal with the main switch and it is free from additional gate driver. The additional winding is implemented in the preexisting transformer and does not require another magnetic core. This idea was firstly proposed and generalized for a several isolated converters in [25]. The work in [26] adds extra switch to the secondary side of the flyback converter, and gains bidirectional power flow and enlarges its range of application.

This paper, as the extension of [25], shows refined analysis and experimental results for the proposed flyback rectifier: in Section II, circuit structure and operation principles of the proposed flyback rectifier are explained. Also, the semiconductor losses in both the proposed and conventional flyback rectifiers are mathematically derived and compared to each other. Section III focuses on designing the proposed circuit, especially on transformer windings turns ratio and snubber configurations. Experimental results shown in Section IV verify the higher efficiency of the proposed rectifier than the conventional one, and Section V concludes the paper.

II. Proposed Bridgeless Flyback Rectifier

A. Circuit Structure and Operation

Fig. 1 compares the two circuits: the conventional flyback rectifier with the bridge diodes and the proposed bridgeless one. As shown in Fig. 1(b), the proposed rectifier eliminates the bridge diodes at the input side, $D_{\rm bd}$ in Fig. 1(a), and minimizes the conduction loss on the primary side. Considering that the general bridgeless rectifiers cannot remove all four bridge diodes for reverse voltage or current blocking [21]–[24] and common mode noise reduction [20], the proposed circuit does not need any diode at all and further reduces the conduction loss.

A few more circuit components are added to the proposed flyback rectifier as the tradeoff of eliminating four bridge diodes. However, the addition should be minimal because it generally increases the circuit complexity. Fig. 1(b) presents the proposed flyback rectifier: a switch on the primary side, S_2, a diode on the secondary side, D_2, and the additional winding, N_{33}, are newly added compared with the conventional circuit in Fig. 1(a). These components give minimum effect to the circuit simplicity of the proposed circuit to secure the inherent advantage of the flyback converter, i.e., simple structure and low cost.

S_2 shares its source terminal and gate signal with S_1 so that additional gate driver is not necessary. Adding D_2 to the secondary side reduces the average current stress of both D_1 and D_2: output diode current in the conventional rectifier, $i_{\rm D0}$ in Fig. 1(a), is divided into $i_{\rm D1}$ and $i_{\rm D2}$ in the proposed rectifier in Fig. 1(b) according to the line voltage polarity. The divided output current makes the heat management of D_1 and D_2 easier than that of D_0. In addition, D_1 and D_2 can be in single semiconductor package if a three-pin center-tapped device with proper current rating is used, which further simplifies the circuit structure. N_{33} has the same turn number with N_{22}, and occupies negligible area in the printed circuit board because it is physically inside the transformer and connected to the pins which are already included in the transformer footprint. Generally, the secondary winding has smaller number of turns than the primary one in the flyback rectifier transformer, and the addition of N_{33} has therefore negligible effect on the transformer core size. In other words, it is easier to add another secondary winding to the transformer than to add extra primary winding as in [24].

The proposed converter may be compared with the flyback converter with the synchronous rectifier (SR) [29] on its secondary side because the two circuits improve their efficiency in the same way: replace the diode in the conduction path into a MOSFET. If the SR is implemented to be self-driven, however, the converter will suffer from the turn-off delay of SR because it may cause overshoot current [30]. And if the SR is driven by complementary gate signal with the primary side switch, the circuit should use extra signal isolation and it makes the circuit more complicated. The proposed circuit is free from the aforementioned problems of the SR.

The proposed rectifier operates in constant-duty fixed-frequency DCM controlled by a simple low-bandwidth voltage loop. The operation acquires high PF and low current distortion without any current control, because the average switch current $i_{\rm S12}$ per switching period is naturally proportional to the instantaneous line voltage $v_{\rm in}$ [1].

Assuming that the transformer has zero leakage inductance and the semiconductor devices have negligible on-state resistance and forward voltage drop, the proposed rectifier has six equivalent topological states in the steady-state operation according to the line voltage polarity and switching state as shown in Fig. 2. L and i_L are the transformer magnetizing inductance and its current, respectively. The states are highly similar to the conventional flyback converter. States 1 to 3 from Fig. 2(a) to

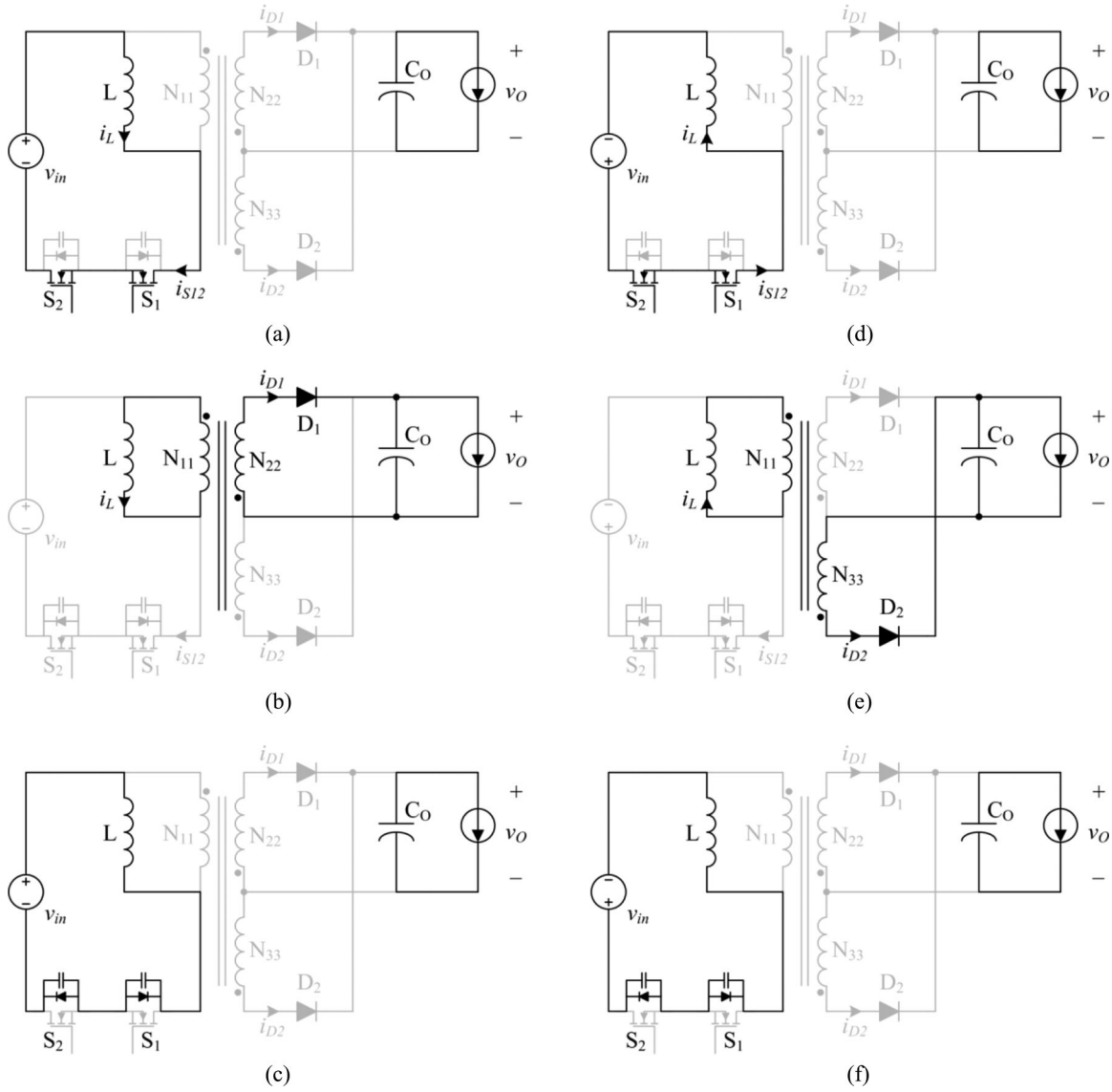

Fig. 2. Six operational states of the proposed flyback rectifier: (a) state 1, (b) state 2, (c) state 3, (d) state 4, (e) state 5, and (f) state 6.

(c) occur when the line voltage $v_{\rm in}$ is positive. N_{33} and D_2 do not participate in the rectifier operation and conduct no current. In state 1, S_1 and S_2 turn ON and the positive $v_{\rm in}$ stores energy in L. $i_{\rm L}$ and $i_{\rm S12}$ increase linearly and the output capacitor C_O supplies power to the load. A transformer design criterion such as (24) should be met to avoid the unexpected turn-on of D_2, which will be articulated in Section III. When S_1 and S_2 turn OFF at the beginning of state 2, the energy in L is transferred to C_O and load through N_{22} and D_1. State 3 starts when $i_{\rm L}$ decreases and touches zero. Parasitic capacitances of S_1 and S_2 resonate with L. States 4 to 6 in Fig. 2(d)–(f) occur when $v_{\rm in}$ is negative. They are similar with the states 1 to 3, except that $i_{\rm Lm}$ and $i_{\rm S12}$ have the opposite direction and N_{33} and D_2 operate instead of N_{22} and D_1. Key waveforms of the proposed rectifier as well as $i_{\rm S0}$ of the conventional rectifier are in Fig. 3.

If the proposed rectifier operates in a continuous conduction mode (CCM), states 3 and 6 will not occur and states 1, 2, 4, and 5 will alternate according to the line voltage polarity.

B. Conduction and Switching Loss Analysis in the Primary Side Switch

The proposed flyback rectifier shows higher efficiency than the conventional one due to the conduction loss reduction on the primary side. The two diodes on the secondary side share the average current and relieve the thermal stress, but their conductions losses are effectively the same as the conventional rectifier. In this section, both the conduction and switching loss on the primary side of the rectifiers are analyzed.

1) Conduction Loss Analysis: The primary side current of the proposed rectifier, $i_{\rm S12}$ in Fig. 1(b), flows through two MOSFETs, while the current in the conventional one, $i_{\rm S0}$ in Fig. 1(a), experiences three: two bridge diodes and one MOSFET. $i_{\rm S12}$ and $i_{\rm S0}$ have the same waveform as each other except their polarities as displayed in Fig. 3, because the proposed and conventional rectifiers utilize similar topology and same control loop. To estimate and compare the conduction losses in the diode and switch, average and root-mean-square

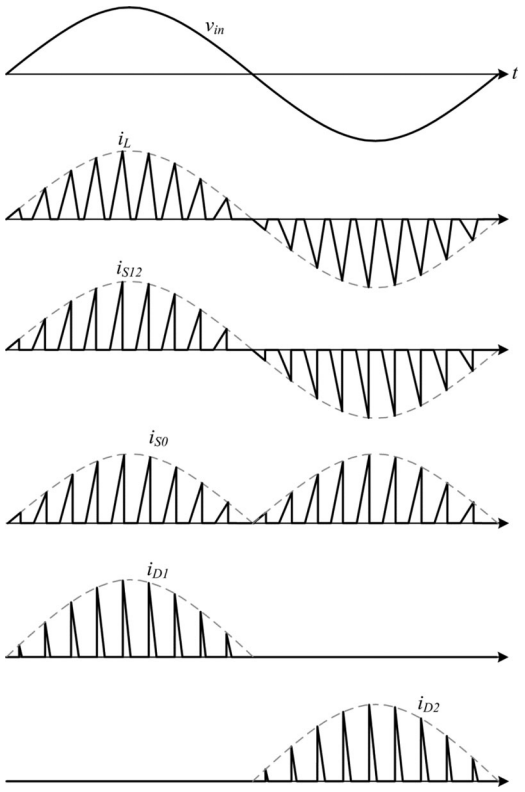

Fig. 3. Key waveforms of the proposed flyback rectifier and i_{S0} of the conventional rectifier during a line cycle.

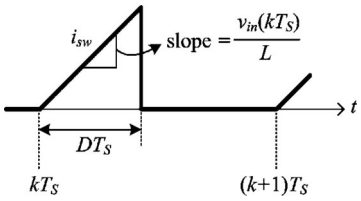

Fig. 4. Switch current of the DCM flyback rectifier in a unit switching period.

(rms) of these primary currents within a half-line cycle are calculated. The rectifier is assumed to operate in the steady-state fixed-frequency DCM with virtually constant duty cycle during a half-line cycle to simplify the analysis.

To calculate the average current in a half-line cycle, average current in a switching period should be derived first. According to the waveform in Fig. 4, the average current in the kth switching period $\langle i_{\rm sw}(kT_S)\rangle_{T_S}$ is determined as follows:

$$\langle i_{\rm sw}(kT_S)\rangle_{T_S} = \frac{1}{T_S}\int_{kT_S}^{(k+1)T_S} i_{\rm sw}(\tau)d\tau = \frac{1}{T_S}\int_0^{DT_S} \frac{v_{\rm in}(kT_S)}{L}\tau d\tau = \frac{v_{\rm in}(kT_S)}{2L}D^2T_S \tag{1}$$

where $i_{\rm sw}(t)$, T_S, and D are absolute values of i_{S0} and i_{S12}, switching period, and duty cycle, respectively. The sinusoidal input voltage $v_{\rm in}$ defined in (2) is treated as a constant in the integration in (1) because its change during a switching cycle is negligible

$$v_{\rm in}(t) = V_{\rm in}\sin\omega_L t. \tag{2}$$

ω_L in (2) is the line voltage angular frequency. Average current in a half-line cycle $\langle i_{\rm sw}\rangle_{T_{\rm ac}}$ is defined as in (3):

$$\langle i_{\rm sw}\rangle_{T_{\rm ac}} = \frac{1}{T_{\rm ac}}\sum_{k=0}^{\left\lfloor \frac{T_{\rm ac}}{T_S}\right\rfloor} \langle i_{\rm sw}(kT_S)\rangle_{T_S} T_S \tag{3}$$

where $T_{\rm ac}$ is a half-line cycle period which is in relationship with ω_L as follows:

$$T_{\rm ac} = \frac{\pi}{\omega_L}. \tag{4}$$

If a half-line period includes m switching periods, i.e., $T_{\rm ac} = mT_S$, and m is sufficiently large, the summation in (3) is approximated into a definite integral as expressed in

$$\langle i_{\rm sw}\rangle_{T_{\rm ac}} \cong \lim_{m\to\infty}\frac{1}{T_{\rm ac}}\sum_{k=0}^{m-1}\langle i_{\rm sw}(kT_S)\rangle_{T_S}T_S = \frac{1}{T_{\rm ac}}\int_0^{T_{\rm ac}}\langle i_{\rm sw}(\tau)\rangle_{T_S}d\tau. \tag{5}$$

Substituting (1) and (2) into (5) and rearranging the terms yield

$$\langle i_{\rm sw}\rangle_{T_{\rm ac}} = \frac{V_{\rm in}}{\pi L}D^2T_S. \tag{6}$$

The primary side rms current during a half-line period is defined in the following:

$$i_{{\rm rms},T_S} = \sqrt{\frac{1}{T_{\rm ac}}\int_0^{T_{\rm ac}} i_{\rm sw}^2(\tau)d\tau}. \tag{7}$$

The integral term in (7) is expanded as the sum of integrals over one switching cycle as shown in the following:

$$\int_0^{T_{\rm ac}} i_{\rm sw}^2(\tau)d\tau = \sum_{k=0}^{m-1}\int_{kT_S}^{(k+1)T_S} i_{\rm sw}^2(\tau)d\tau \tag{8}$$

assuming $T_{\rm ac} = mT_S$. Integral of $i_{\rm sw}^2$(t) over the kth switching cycle is as follows:

$$\int_{kT_S}^{(k+1)T_S} i_{\rm sw}^2(\tau)d\tau = \int_0^{DT_S}\left(\frac{v_{\rm in}(kT_S)}{L}\right)^2\tau^2 d\tau = \frac{1}{3}\left(\frac{v_{\rm in}(kT_S)}{L}\right)^2 D^3T_S^3. \tag{9}$$

$v_{\rm in}$ in (9) is also treated as a constant, similar as in (1). Equation (8) is alternatively expressed as in (10) by considering (9):

$$\int_0^{T_{\rm ac}} i_{\rm sw}^2(\tau)d\tau = \sum_{k=0}^{m-1}\frac{1}{3}\left(\frac{v_{\rm in}(kT_S)}{L}\right)^2 D^3T_S^3. \tag{10}$$

The assumption that T_S is much smaller than $T_{\rm ac}$ and m is sufficiently large, which was previously used in achieving (5),

approximates (10) into (11)

$$\int_0^{T_{\rm ac}} i_{\rm sw}^2(\tau)d\tau \cong \lim_{m\to\infty}\sum_{k=0}^{m-1}\frac{1}{3}\left(\frac{v_{\rm in}(kT_S)}{L}\right)^2 D^3T_S^3 = \int_0^{T_{\rm ac}}\frac{1}{3}\left(\frac{v_{\rm in}(\tau)}{L}\right)^2 D^3T_S^2 d\tau. \quad (11)$$

Substituting (2) into (11) yields

$$\int_0^{T_{\rm ac}} i_{\rm sw}^2(\tau)d\tau = \frac{D^3T_S^2}{6L^2}V_{\rm in}^2T_{\rm ac} \quad (12)$$

and substituting (12) into (7) derives the primary side rms current over a half-line period as shown in the following:

$$i_{{\rm rms},T_S} = \sqrt{\frac{1}{T_{\rm ac}}\frac{D^3T_S^2}{6L^2}V_{\rm in}^2T_{\rm ac}} = \frac{T_SV_{\rm in}}{L}\sqrt{\frac{D^3}{6}}. \quad (13)$$

The conduction loss of a bridge diode, P_D, is estimated by using (6) such as in

$$P_D = \langle i_{\rm sw}\rangle_{T_{\rm ac}} v_F \quad (14)$$

and that of a MOSFET, $P_{\rm sw}$, is by using (13) as in the following:

$$P_{\rm sw} = i_{{\rm rms},T_S}^2 r_{\rm ds} \quad (15)$$

where v_F and $r_{\rm ds}$ are forward voltage drop of the bridge diode and on-state resistance of the MOSFET, respectively. The primary side conduction losses in the semiconductor devices in the conventional and proposed rectifiers, $P_{\rm conv}$ and $P_{\rm prop}$ respectively, are defined in (16) and (17) according to the number of the diodes and MOSFETs

$$P_{\rm conv} = 2P_D + P_{\rm sw} \quad (16)$$

$$P_{\rm prop} = 2P_{\rm sw}. \quad (17)$$

Considering (6), (13)–(17), and D in the steady-state operation defined in (18), $P_{\rm conv}$ and $P_{\rm prop}$ are the function of output power P_O and peak line voltage $V_{\rm in}$

$$D = \frac{2}{V_{\rm in}}\sqrt{\frac{LP_O}{T_S}}. \quad (18)$$

Fig. 5 compares the calculated $P_{\rm conv}$ and $P_{\rm prop}$ in a three-dimensional plot when L, T_S, v_F, and $r_{\rm ds}$ are 370 μH, 25 μs (reciprocal of 40 kHz), 1.1 V, and 0.6 Ω, respectively. $P_{\rm conv}$ surface is higher than $P_{\rm prop}$ in any operation condition, which means the proposed rectifier always demonstrates lower conduction loss than the conventional one. Curves in Figs. 6 and 7 are the cut ends of the planes in Fig. 5 in the x- and y-axes direction. Fig. 6 depicts that the more conduction loss is reduced when the output power is higher, because the differences between the solid and broken lines are larger in heavier load. Similar fact is noticed in Fig. 7 that the loss reduction of the proposed topology is more effective in lower line voltage, providing the same output power. Also, the curves in Fig. 7 show that the proposed rectifier may not be helpful to improve the efficiency in higher power, i.e., in the range not shown in the x-axis of Fig. 7. It is because the curves of the proposed rectifier increase steeper than those of the conventional one and go beyond them as the output power increases. Indeed, the proposed topology is beneficial in the loss reduction in the power range where the flyback converters are widely used.

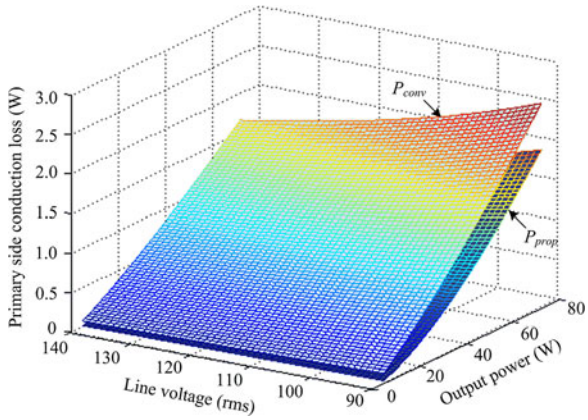

Fig. 5. Calculated primary side conduction losses of the two rectifiers as the function of the line voltage and output power according to (16) and (17).

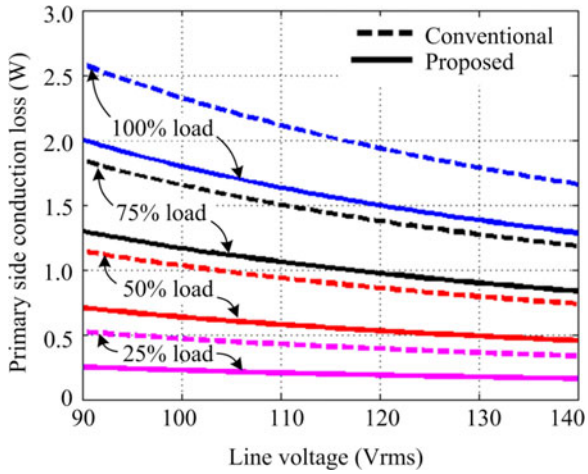

Fig. 6. Calculated primary side conduction losses according to the line voltage.

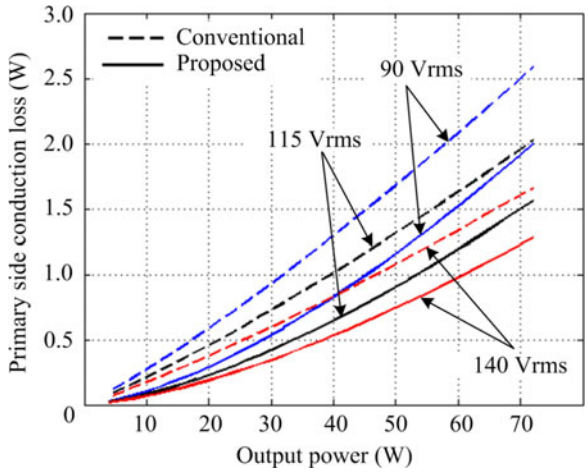

Fig. 7. Calculated primary side conduction losses according to the output power.

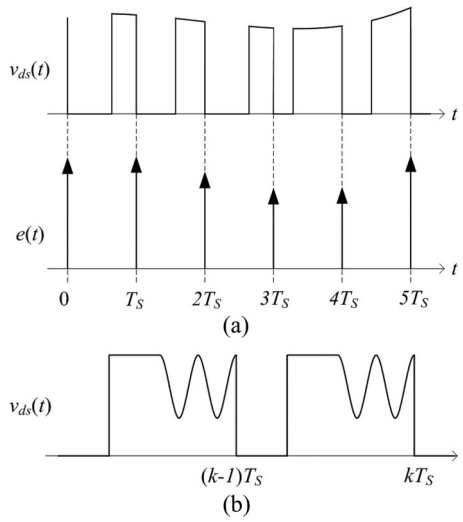

Fig. 8. (a) Voltage and energy waveforms of the MOSFET parasitic output capacitance. (b) The worst case turn-on of the MOSFET in DCM operation.

2) Switching Loss Analysis: The switching loss of a MOSFET is determined by the energy dissipated from its parasitic output capacitances $C_{\rm oss}$, and the energy is generated in a discrete way, as synchronized with the turn-on instant as shown in Fig. 8. In Fig. 8(a), $v_{\rm ds}(t)$ and $e(t)$ are the voltage across MOSFET and the instantaneous energy dissipated from the capacitance, respectively. The energy is dissipated once in a switching period and thus shown as a series of weighted delta functions. Power is the sum of energy divided by a certain time interval by definition, and the switching loss P_S caused by $C_{\rm oss}$ during n switching periods is as expressed in

$$P_S = \frac{1}{mT_S}\sum_{k=1}^{m-1}\frac{1}{2}C_{\rm oss}v_{\rm ds}(kT_S)^2. \tag{19}$$

The summation in (19) is the total energy dissipated from the capacitance during a half-line cycle.

In DCM, however, it is not straightforward to predict $v_{\rm ds}(kT_S)$ at turn-on instant because $C_{\rm oss}$ and the leakage inductance resonate before the turn-on. In this paper, the MOSFET is assumed to be turned ON in the worst case in every switching period, i.e., $v_{\rm ds}$ is the maximum at kT_S as shown in Fig. 8(b). It is not the precise calculation in practice, but can be used as the conservative design limit.

Considering $v_{\rm ds}(t)$ is determined as in (20) according to the worst case assumption and the flyback converter topology, (19) becomes as in (21)

$$v_{\rm ds}(t) = V_{\rm in}\sin\omega_L t + nV_O \tag{20}$$

$$P_S = \frac{1}{mT_S}\sum_{k=1}^{m-1}\frac{1}{2}C_{\rm oss}\left(V_{\rm in}\sin\omega_L kT_S + nV_O\right)^2. \tag{21}$$

In (20) and (21), V_O represents the steady-state output voltage. Applying the same assumption used in (5) and (11) and some mathematical manipulation, P_S is expressed as

$$P_S \cong \lim_{m\to\infty}\frac{1}{mT_S^2}\sum_{k=1}^{m-1}\frac{1}{2}C_{\rm oss}\left(V_{\rm in}\sin\omega_L kT_S + nV_O\right)^2 T_S$$

$$= \frac{C_{\rm oss}}{2mT_S^2}\int_0^{T_{\rm ac}}\left(V_{\rm in}\sin\omega_L\tau + nV_O\right)^2 d\tau. \tag{22}$$

Solving the integral in (22) achieves the following equation:

$$P_S = \frac{C_{\rm oss}}{2T_S}\left(\frac{1}{2}V_{\rm in}^2 + \frac{4}{\pi}nV_O V_{\rm in} + n^2V_O^2\right). \tag{23}$$

Though the term in the parentheses in (23) may not be precise in the practical DCM operation, it is obvious from (23) that the higher switching frequency generates the higher switching loss. In this paper, the switching frequency is selected as 40 kHz to compromise the conduction loss and circuit size. It should also be noted that the conventional and proposed rectifiers have the same switching losses as each other, because only one of S_1 and S_2 turns on and off in the proposed rectifier.

III. Design of the Proposed Rectifier

A. Transformer Design

Transformer has two design parameters which are directly related to the flyback rectifier operation and performance: turns ratio of windings, n, and the magnetizing inductance, L. The only design condition for L is to make it smaller than a certain value not to operate the rectifier in unexpected CCM [1], [25].

The secondary side windings N_{22} and N_{33} have the same number of turns to make the voltage gains and frequency responses the same for any line voltage polarities. n, defined as $n:1:1 = N_{11}:N_{22}:N_{33}$, has the lowest limit as shown in the following equation:

$$n > \frac{V_{\rm in\,max}}{V_O}. \tag{24}$$

$V_{\rm in\,max}$ indicates the instantaneous maximum line voltage in (24). The inequality in (24) is mandatory not to short out the transformer during the freewheeling states. For example, D_1 and D_2 should not conduct any current in state 1 [see Fig. 2(a)]. If (24) is not met, D_2 will conduct undesirably because the voltage across D_2 is not sufficient to reverse-bias it. The two voltage sources, $v_{\rm in}$ and V_O, are then effectively connected in parallel and excessive current may flow in the rectifier. In similar way, D_1 may turn ON in state 5 unexpectedly [see Fig. 2(d)] if (24) is not satisfied.

n also has the highest limit according to the voltage rating of the MOSFETs on the primary side. Practically, the MOSFET should secure some voltage margin than the voltage stress in ideal case, because the transformer leakage inductance and the parasitic capacitances incurs voltage spike across it. Equation (25) mathematically expresses this condition

$$V_{\rm ds\,max} > V_{\rm in\,max} + n\left(K+1\right)V_O \tag{25}$$

where $V_{\rm ds\,max}$ is the rated voltage of the MOSFET and K is a design constant for snubber which is generally determined between 1 and 2, i.e., $1 < K < 2$. Rearranging (25) for n and

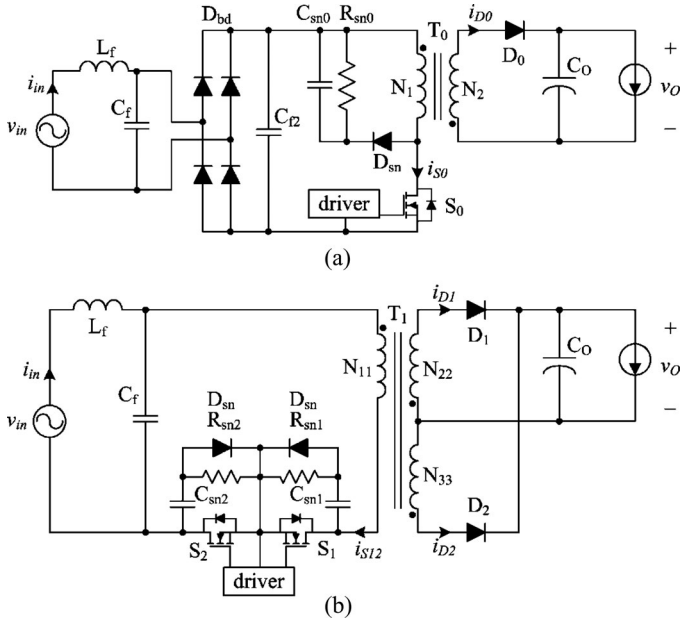

Fig. 9. Experimental setup of (a) conventional and (b) proposed flyback rectifiers.

merging with (24) achieve (26):

$$\frac{V_{\text{in max}}}{V_O} < n < \frac{V_{\text{ds max}} - V_{\text{in max}}}{(K+1)\,V_O}. \tag{26}$$

B. Snubber Design

The rectifiers in this paper utilize passive resistor–capacitor–diode (RCD) snubbers to minimize the number of active switches and simplify the circuit structure. For the proposed rectifier, conventional RCD snubber shown in [11] cannot be applied because it does not operate properly when the line voltage is negative in the bridgeless circuit configuration. Instead, other RCD snubber configuration presented in [27] and utilized in [28] is applied to each MOSFET device. These snubbers are directly implemented to the switch devices, i.e., connected to the drain and source terminals of the MOSFET [shown in Fig. 9(b)], and are not affected by other circuit configurations such as input voltage polarity.

IV. Experimental Results

A. Implementation

For experimental verification, the proposed and conventional flyback rectifiers are built and tested. Fig. 9 shows the implementation of the two rectifiers. They are constructed by using the same circuit elements and parameters for fair comparison, which are listed as follows:

1) v_{in}: 90–140 V_{rms}, 60 Hz, given by power supply Kikusui PCR2000L;
2) output power in full load: 72 W, consumed by electric load Prodigit 3361F;
3) V_O: 48 V;
4) T_S: 25 μs;
5) L_f: 250 μH;
6) C_f: 1μF;
7) D_{bd}: D15XB60;
8) C_{f2}: 330 nF;
9) C_{sn0}: 20 nF;
10) R_{sn0}: 100 kΩ;
11) D_{sn}: 1N5407;
12) S_0, S_1, S_2: FQA13N80 (800 V, 8 A);
13) T_0, T_1: PQ26/25 with PC44 material manufactured by TDK, magnetizing inductances 370 μH;
14) N_1: N_2 = 40:8;
15) N_{11}: N_{22}: N_{33} = 40:8:8 (not abbreviated but actual number of turns);
16) D_0, D_1, D_2: RURG3020CC (200 V, 30 A);
17) C_O: 1.98 mF (six 330 μF/63 V electrolytic capacitors parallel)
18) R_{sn1}: 130 kΩ;
19) R_{sn2}: 350 kΩ;
20) $C_{\text{sn1}}, C_{\text{sn2}}$: 4.4 nF;
21) Controller IC: Microchip dsPIC33FJ16GS502.

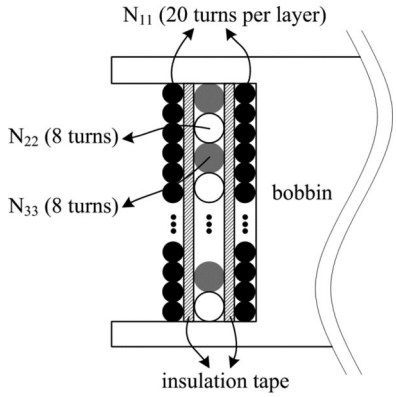

Fig. 10. Winding configuration of T_1 in the proposed rectifier.

It should be noted that v_{in} is not universal, i.e., 90–264 V_{rms}, to meet (25) with practical 800-V rated MOSFET. Though using high-voltage device such as IGBT (insulated gate bipolar transistor) or silicon carbide device may allow the universal line voltage to the proposed circuit, implementation in this paper is focused on comparing the efficiencies of the rectifiers composed of cost-effective circuit elements. The output diodes D_1 and D_2 can be in a single semiconductor package as explained in Section II-A, but they are implemented in separate two packages in this experiment for fair comparison with the conventional rectifier. The capacitance of C_O is designed to be pretty larger than typical value to minimize the equivalent series resistance and output voltage ripple. Input power of the rectifiers is measured by a power analyzer Yokogawa WT210. The voltage control loop is realized by a digital algorithm in the controller IC to have approximately 5–10 Hz bandwidth.

Winding configuration of T_1 for N_{11}, N_{22}, and N_{33} is shown in Fig. 10. N_{22} and N_{33} form bifilar winding in the second layer and covered by N_{11} in the first and the third layers to minimize the leakage inductance and maximize the coupling

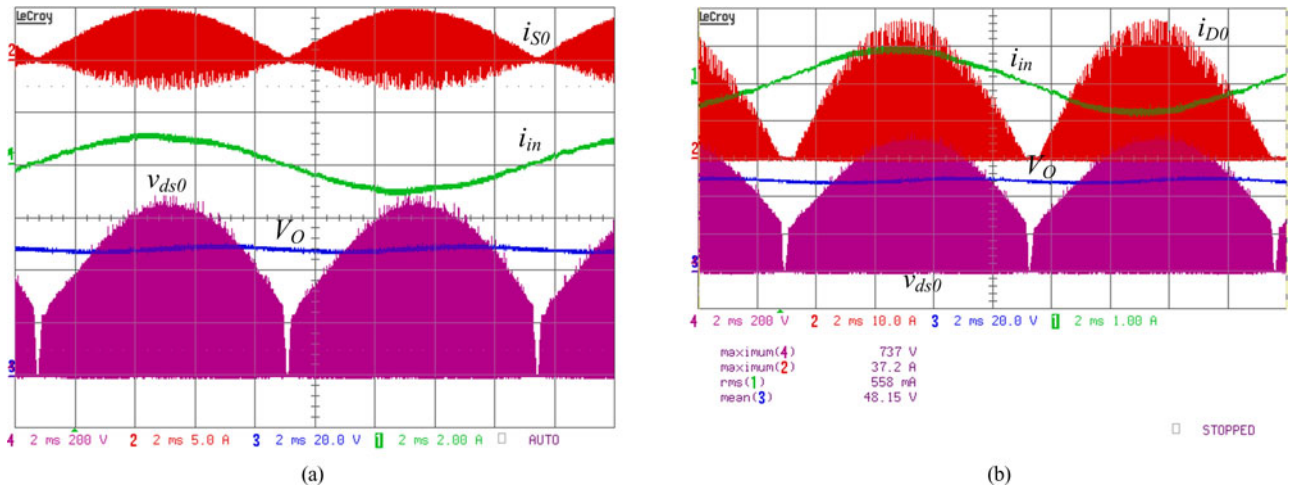

Fig. 11. Experimental waveform of the conventional flyback rectifier in Fig. 9(a). (a) $v_{\rm in}$ is 115 $V_{\rm rms}$ and load is 60%. ($i_{\rm S0}$: 5 A/div., $i_{\rm in}$: 2 A/div., $v_{\rm ds0}$: 200 V/div., V_O: 20 V/div., 2 ms/div.) (b) $v_{\rm in}$ is 140 $V_{\rm rms}$ and load is 100%. ($i_{\rm D0}$: 10 A/div., $i_{\rm in}$: 1 A/div., $v_{\rm ds0}$: 200 V/div., V_O: 20 V/div., 2 ms/div.)

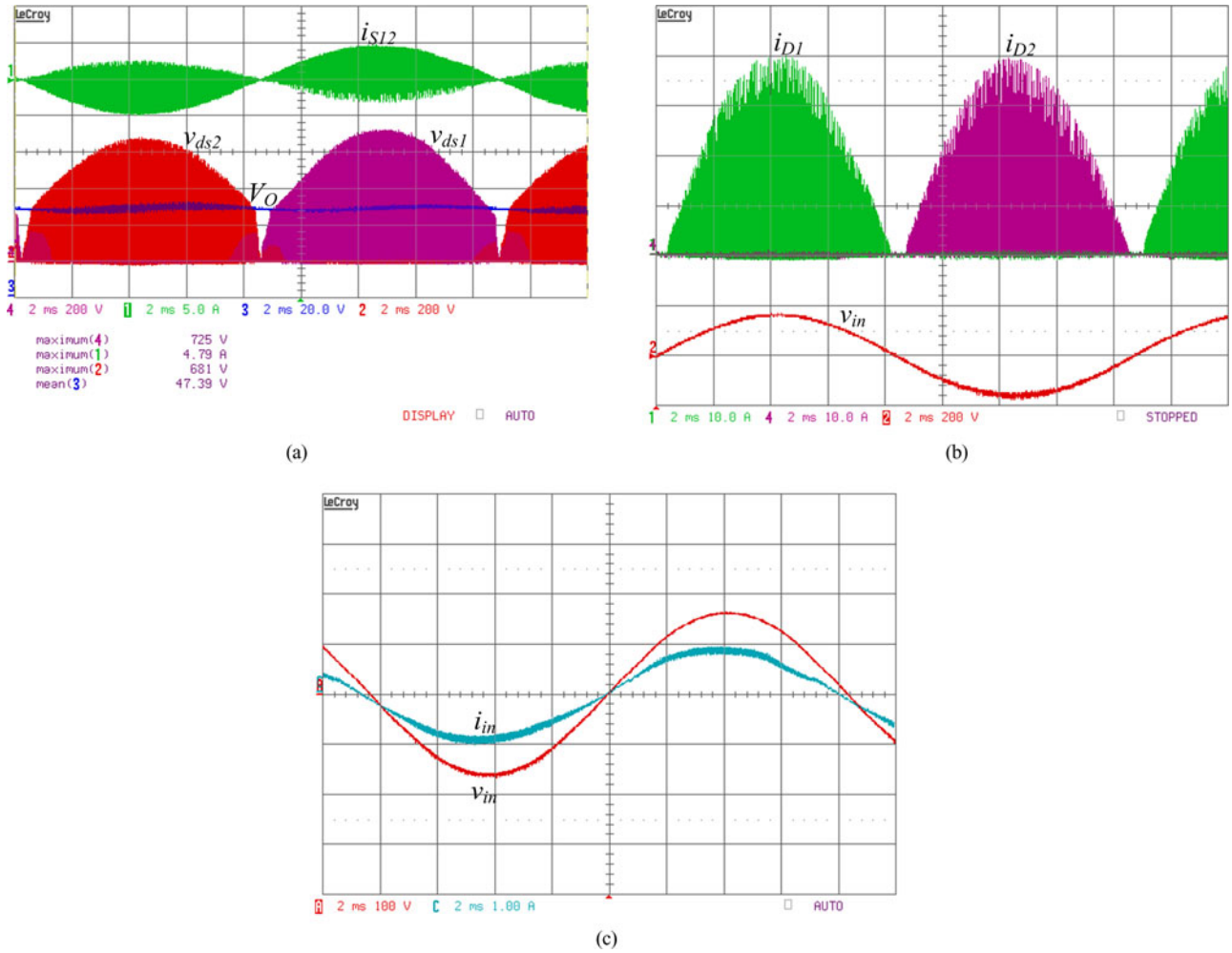

Fig. 12. Experimental waveforms of the proposed flyback rectifier in Fig. 9(b). (a) 140-$V_{\rm rms}$ input voltage and 100% load operation ($i_{\rm S12}$: 5 A/div., $v_{\rm ds1}$ and $v_{\rm ds2}$: 200 V/div., V_O: 20 V/div., 2 ms/div.) (b) 115-$V_{\rm rms}$ input voltage and 100% load operation (i_{D1} and i_{D2}: 10 A/div., $v_{\rm in}$: 200 V/div., 2 ms/div.) (c) 115-$V_{\rm rms}$ input voltage and 100% load operation ($i_{\rm in}$: 1 A/div., $v_{\rm in}$: 100 V/div., 2 ms/div.)

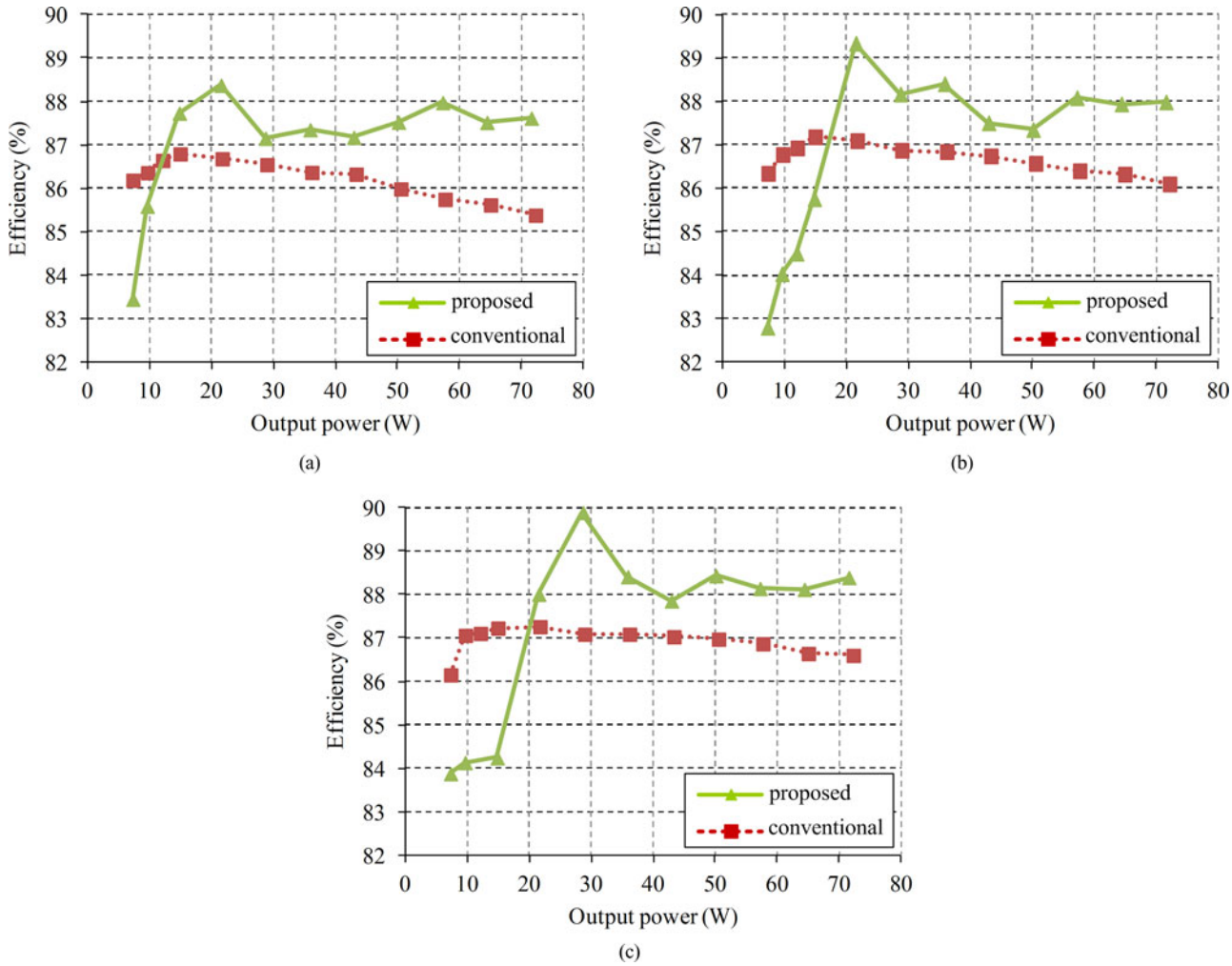

Fig. 13. Efficiency comparison of the two rectifiers when $v_{\rm in}$ is (a) 90 $V_{\rm rms}$, (b) 115 $V_{\rm rms}$, and (c) 140 $V_{\rm rms}$.

coefficient. Also, it is important to place N_{22} and N_{33} as close as possible to achieve the uniform coupling with N_{11}. If the coupling coefficient between N_{11} and N_{22} is different from that between N_{11} and N_{33}, the transformer will have different effective turns ratio for each line voltage polarity and the output voltage will have twice line-frequency fluctuation.

The snubber for the conventional rectifier configured by $R_{\rm sn0}, C_{\rm sn0}$, and $D_{\rm sn}$ is designed by the steps shown in [11] and tuned to clamp the drain–source voltage of S_0 down to 737 V in the worst case, i.e., maximum line voltage and full load condition [see Fig. 11(b)]. The snubbers for the proposed rectifier are also tuned to clamp S_1 and S_2 voltage to 725 V and 680 V [see Fig. 12(a)]. The snubbers for each switch should have the same resistors and capacitors in ideal case, but they are not in practical implementation: it is because the common mode parasitic capacitance affects the resonance between the leakage inductance and switch output capacitances when the line voltage is negative. Though the clamped MOSFET voltages in the two rectifiers are not exactly the same to each other, it does not exaggerate the proposed circuit efficiency and mislead the efficiency comparison because lower clamped voltage causes more heat dissipation in the snubber resistor.

B. Experimental Results

Fig. 11(a) shows the experimental waveform of the conventional rectifier in Fig. 9(a) when $v_{\rm in}$ is 115 $V_{\rm rms}$ and output load is 60%. The line current, $i_{\rm in}$, is the filtered version of the switch current $i_{\rm S0}$ by the line filter, and it is close to the pure sine wave. The average $i_{\rm S0}$ during a switching cycle is always positive regardless of the line voltage polarity due to the rectifying operation of the bridge diodes. The drain–source voltage of $S_0, v_{\rm ds0}$, is switching in both positive and negative half-line periods, which is also due to the bridge diodes. Fig. 11(b) shows that the snubber limits the maximum $v_{\rm ds0}$ in the conventional flyback rectifier to 737 V in the worst case operation, i.e., the maximum instantaneous input voltage and full load condition. The voltage 737 V is referenced in the snubber design for the proposed rectifier.

Operation of the proposed flyback rectifier in Fig. 9(b) is exhibited in Fig. 12. Fig. 12(a) presents the switch current $i_{\rm S12}$, drain–source voltages of S_1 and $S_2, v_{\rm ds1}$ and $v_{\rm ds2}$, respectively, and output voltage V_O when the rectifier operates in 140-$V_{\rm rms}$ line voltage and 100% load condition. Comparing $v_{\rm ds0}$ in Fig. 11(a), $v_{\rm ds1}$ and $v_{\rm ds2}$ alternatively experience

the voltage stress according to the polarity of $v_{\rm in}$. $i_{\rm S12}$ has the similar shape as $i_{\rm S0}$ in Fig. 11 but its polarity follows the line voltage polarity. V_O is controlled as 48 V which is the same level with that presented in Fig. 11. Output diodes D_1 and D_2 carry currents alternatively according to the sign of $v_{\rm in}$, as $i_{\rm D1}$ and $i_{\rm D2}$ show in Fig. 12(b) when $v_{\rm in}$ is 115 $V_{\rm rms}$ and load is 100%. They have the same magnitude as each other because N_{22} and N_{33} have the same number of turns. Fig. 12(c) is captured in the same operation condition with Fig. 11(b), and proves that the line current $i_{\rm in}$ of the proposed rectifier is sinusoidal and synchronized to $v_{\rm in}$ to achieve high PF and low distortion.

Fig. 13 compares the efficiency of the two rectifiers for various line voltages. The proposed rectifier has higher efficiency by 0.5–3% than the conventional one in medium and high load range, where the conduction losses dominate the switching losses. The proposed circuit shows especially high efficiency in 30-W load regardless of the line voltage magnitude, and the maximum efficiency improvement occurs at 140-$V_{\rm rms}$ input and 30-W operation as shown in Fig. 13(c). Though the input line voltage range is limited by the voltage rating of the MOSFET, the proposed circuit indeed features high efficiency than the conventional one in the low line voltage application.

The lower efficiency of the proposed rectifier in the light load range is due that the snubber loss of the proposed rectifier is slightly higher than that of the conventional one. The intersection of the two efficiency curves in Fig. 13(a)–(c) occurs at 12 W, 18 W, and 20 W approximately, i.e., at the higher output power when the higher line voltage is applied. This is because the efficiency improvement from the primary side conduction loss saves smaller power in the high input voltage application as shown in Figs. 5 and 7, while the snubber loss in the proposed circuit is virtually constant.

V. Conclusion

A modified PFC flyback rectifier for ac–dc conversion has been proposed in this paper. The circuit is derived from conventional flyback rectifier by removing all four bridge diodes and adding a switch on the primary side and a diode-winding pair on the secondary side. The addition of these elements does not affect the circuit complexity much, because the additional switch and winding do not need extra gate driver and magnetic core. The reduced number of the semiconductor devices on the primary side saves the conduction loss and improves the rectification efficiency. According to the mathematical derivation, the topology saves more conduction loss in higher output power and lower line voltage condition. The experimental results based on the prototype rectifiers have proved that the proposed flyback circuit shows higher efficiency than its conventional counterpart in the medium and heavy load range.

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